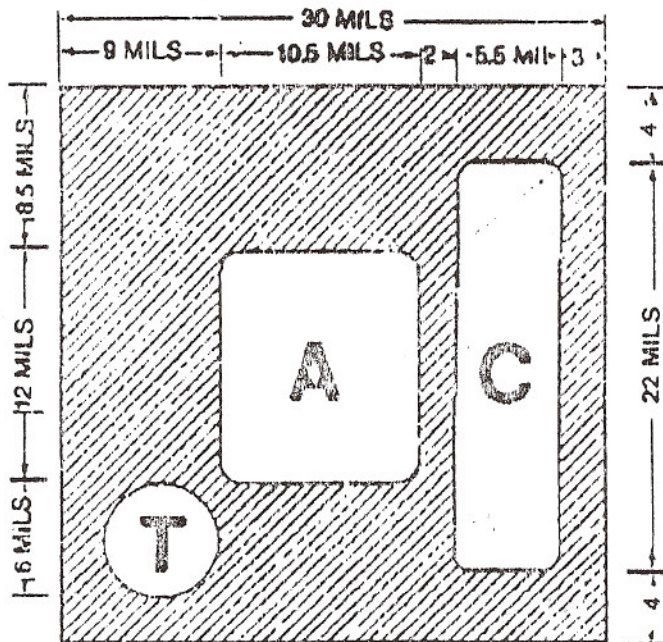




Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Backside is not cathode and must be electrically isolated.

Topside Metal:
Backside: Au
Backside Potential: See Above
Mask Ref:
Bond Pads (Mils): See Above

APPROVED BY:
MFG: CDI

DIE SIZE (Mils): 30 x 30
THICKNESS:

DATE: 9/2/99
P/N: CD4578